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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,321	10/31/2003	Stewart Logie	10069/26	2545

7590 03/30/2005

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/699,321	LOGIE, STEWART	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-7,11-13,15,16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-7,11-13,15,16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's Amendment filed 03/14/05 is acknowledged. Upon further consideration by the Examiner, pertinent prior art was found that reads on Applicant's pending claims. A new rejection follows. The finality of the office action mailed 12/14/04 is withdrawn.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravanelli (U.S. Patent No. 5,959,332) in view of Ker et al. (U.S. Patent No. 6,750,515 B2).

In re claim 4, Ravanelli (esp. Fig. 1) discloses a semiconductor device, comprising:

a substrate (P body) having a first junction region (18) separated from a second junction region (20) by a substrate region;

an MOS gate electrode overlying the substrate region and separated therefrom by a gate oxide layer;

dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

wherein the substrate region is defined by a uniformly doped region of the substrate between the first junction region and second junction region, and

wherein the first junction region (18) comprises an anode and the second junction region (20) comprises a cathode, and wherein the anode and the cathode have an opposite conductivity type.

Ravanelli does not expressly disclose sidewall spacers adjacent opposing sides of the MOS gate electrode and overlying the substrate region. Ker (esp. Fig. 3) discloses a MOS gate electrode with sidewall spacers. It would have been obvious to one skilled in the art at the time of the invention to form sidewall spacers as disclosed by Ker for the device of Ravanelli to enhance the formation of lightly doped source/drain regions (14, 15).

In re claim 6, Ravanelli in view of Ker discloses the device of claim 4. The limitation, "wherein the device ... regions" is a recitation of the intended use of the device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 7, Ravanelli in view of Ker discloses the device of claim 4, wherein the gate electrode is electrically coupled to the substrate.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ravanelli in view of Ker as applied to claim 4 above, and further in view of Jun et al. (U.S. Patent No. 6,552,399).

In re claim 5, Ravanelli in view of Ker discloses the device of claim 4, but does not expressly disclose the length of the channel. Jun (esp. Fig. 3a) discloses the use of channel length to achieve various transistor characteristics. It would have been obvious for one skilled in

the art to alter the channel length of Ravanelli/Ker as disclosed by Jun for the purpose, for example, of enhancing the ability to change to voltage of the transistor to protect against ESD events (Jun, column 3, lines 30-38).

4. Claims 11-13, 15, 16 and 18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (U.S. Patent No. 6,552,399 B2) view of Ker et al. (U.S. Patent No. 6,750,515 B2).

In re claim 11 Jun (esp. Fig. 3a) discloses a semiconductor device comprising:

a voltage supply node (34) and a ground node (Ground);

an MOS circuit (with gate 35) coupled to the voltage body supply node and to the ground node;

a transistor (with gate 35) having a first junction region (13) coupled to the voltage supply node, a second junction region (36) coupled to the ground node, and a substrate region between the first and second junction regions;

wherein the substrate region comprises a junction-free semiconductor region between the first and second junction regions; and

wherein the anode (36) and the substrate region (11) comprise a semiconductor material of the same conductivity type; and

an MOS gate electrode (33) overlying the substrate region and separated therefrom by a gate oxide layer.

Jun does not expressly disclose sidewall spacers adjacent opposing sides of the MOS gate electrode and overlying the substrate region. Ker (esp. Fig. 3) discloses a MOS gate electrode with sidewall spacers. It would have been obvious to one skilled in the art at the time of the

invention to form sidewall spacers as disclosed by Ker for the device of Jun to enhance the formation of source/drain regions (14, 15).

The limitation, "wherein the transistor functions as ... anode" is a recitation of the intended use of the claimed device. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

In re claim 12, Jun in view of Ker discloses the device of claim 11, wherein the transistor couples a plurality of 1 to N forward biased diodes connected in series, such that the first junction region of the first diode is coupled to eh voltage supply node and the second junction region of the Nth diode is coupled to the ground node.

In re claim 13, Jun in view of Ker discloses the device of claim 11. The limitation, "wherein the transistor functions ... collector" is a recitation of the intended use of the device that does not further limit the structure of the parent claim.

In re claim 15, Jun in view of Ker discloses the device of claim 11, wherein the source region (13) is coupled to a signal node (34) of an MOS circuit and the drain region (36) is coupled to a ground node of the MOS circuit.

In re claim 16, Jun in view of Ker discloses the device of claim 11, wherein a thickness of the gate dielectric (under gate 35) is substantially the same as a gate (35) thickness of the MOS circuit.

In re claim 18, Jun in view of Ker discloses the device of claim 11. The limitation, "wherein the device ... regions" is a recitation of the intended use of the device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 19, Jun in view of Ker discloses the device of claim 11, wherein the MOS gate electrode is electrically coupled to the substrate.

In re claim 20, Jun in view of Ker discloses the device of claim 11, wherein the substrate region is defined by a uniformly doped region between the source and drain region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

TOM THOMAS
SUPERVISORY PATENT EXAMINER